In the Claims:

Please cancel claims 9-28, without prejudice, and amend claims 1, 2 and 4-8 as follows:

1. (Currently Amended) A semiconductor integrated circuit comprising:

a bias circuit that has a first current source for generating a first current and a load circuit connected in series with the first current source, and that generates a first voltage at a first node that is a connecting node between the first current source and the load circuit;

a second current source that generates a power supply current in accordance with the first voltage;

an internal circuit that has a plurality of first transistors and is connected to said second current source in order to operate the first transistors; and

a correcting circuit that includes a correcting transistor receiving a constant voltage at a gate, and that generates, in accordance with the constant voltage, a correcting current at a second node electrically connected to a drain of the correcting transistor, the second node being electrically connected to the first node, wherein:

a drain of the correcting transistor is connected to each gate of a pair of second transistors forming a first current mirror circuit; and

a drain of one of the second transistors that is not connected to the correcting transistor is connected to the second node.

2. (Currently Amended) ~~The~~A semiconductor integrated circuit ~~according to claim 1, wherein~~comprising:

a bias circuit that has a first current source for generating a first current and a load circuit connected in series with the first current source, and that generates a first voltage at a first node that is a connecting node between the first current source and the load circuit;

a second current source that generates a power supply current in accordance with the first voltage;

an internal circuit that has a plurality of first transistors and is connected to said second current source in order to operate the first transistors; and

a correcting circuit that includes a correcting transistor receiving a constant voltage at a gate, and that generates, in accordance with the constant voltage, a correcting current at a second node electrically connected to a drain of the correcting transistor, the second node being electrically connected to the first node, wherein:

said bias circuit has a reference voltage generator that has

a threshold voltage compensating function for a variation of a threshold voltage of each of the first transistors formed in said internal ~~circuit~~circuit, and

a temperature compensating function for a temperature ~~variation,~~variation;

said reference voltage generator generating a constant reference voltage independently of the temperature variation and the variation of the threshold voltage; and

said bias circuit generates the first voltage in accordance with the reference voltage.

3. (Original) The semiconductor integrated circuit according to claim 2, wherein

the reference voltage generator is a band-gap reference.

4. (Currently Amended) The semiconductor integrated circuit according to ~~claim 1~~claim 2, wherein

the correcting transistor is an nMOS transistor.

5. (Currently Amended) The semiconductor integrated circuit according to ~~claim 1~~claim 2, wherein

the correcting transistor is a pMOS transistor.

6. (Currently Amended) The semiconductor integrated circuit according to ~~claim 1~~claim 2, wherein:

said first current source and said second current source have a ~~second~~third transistor and a ~~third~~fourth transistor respectively whose gates are connected to the first node; and

the ~~second~~third transistor and the ~~third~~fourth transistor constitute a ~~first~~second current mirror circuit.

7. (Currently Amended) The semiconductor integrated circuit according to ~~claim 1~~claim 2, wherein

a drain of the correcting transistor is directly connected to the second node.

8. (Currently Amended) The semiconductor integrated circuit according to ~~claim 1~~claim 2, wherein:

a drain of the correcting transistor is connected to each gate of a pair of fourth transistors constituting a second current mirror circuit; and

a drain of one of the fourth transistors that is not connected to the correcting transistor is connected to the second node.

9-28. (Canceled)